



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/765,931	01/19/2001	Vinodha Ramasamy	10005775-1	7462

7590 03/12/2004
HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

VU, TUAN A

ART UNIT PAPER NUMBER

2124

2

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

h

Office Action Summary

Application No.

09/765,931

Applicant(s)

RAMASAMY ET AL.

Examiner

Tuan A Vu

Art Unit

2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 January 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

1. This action is responsive to the application filed January 19, 2001.

Claims 1-3 have been submitted for examination.

Claim Rejections - 35 USC § 103

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hastings, USPN: 6,206,584 (hereinafter Hastings) in view of Murphy et al., USPN: 5,659,753 (hereinafter Murphy).

As per claim 1, Hastings discloses a method for allocating stack memory for use in conjunction with modification of a block of programming code (e.g. col. 2, lines 55-63) comprising:

identifying a statement allocating stack memory, the statement (e.g. *malloc*, *realloc* - col. 9, line 37 to col. 10, line 43) associated with the block of programming code; identifying parameters associated with the statement (e.g. *status codes*, *local variables* -- col. 9, line 37 to col. 10, line 43 – Note: identifying instruction and status bits used to allocate stack memory is equivalent to identifying parameters associated statement and *malloc()* inherently suggests use of input parameters); and

by using the parameters as inputs, generating new parameters for use in the statement to allocate the stack memory (e.g. *realloc* - col. 9, line 37 to col. 10, line 43 – Note: reallocating memory structures using stack status bits is equivalent to generating new parameters for use in the statement to allocate stack memory).

But Hastings does not explicitly disclose that allocating stack memory is allocation an N number of registers. The concept of stack being organized in stacked registers for associating

Art Unit: 2124

with variables or temporary data storage during code relocation, dynamic binding or iterative execution was a well-known concept in the art of compiling. Murphy, in a method to provide an optimizing compiler using reallocating instructions for memory fault-prevention like Hastings (see Hastings: col. 11, line 32 to col. 12, line 21), discloses allocation instruction and dynamic storage of variables in registers on stack frame (e.g. col. 48, line 29 to col. 49, line 46); i.e. association of dynamic stack allocation with creation of registers. In case Hastings method does not include stack memory in terms of stacked registers, it would have been obvious for an ordinary skill in the art at the time of the invention was made to implement the dynamic re-allocation of stack memory as suggested by Hastings as re-allocation of stacked registers as taught by Murphy, i.e. allocating a N number of registers, because registers are the most efficient means for storing fleeting values and data for use in the execution flow of a program e.g. so as to provide time efficiency to the execution to the dynamic modification of code as by Hastings which can lead to potential delay.

3. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hastings, USPN: 6,206,584 in view of Murphy et al., USPN: 5,659,753, as applied to claim 1, and further in view of Swerre Jarp, "A Detailed Tutorial", CERN-IT Division, Nov 1999 (hereinafter Jarp).

As per claim 2, the combination Hastings/Murphy does not specify parameters identifying a number I input registers, a number L of local registers, and a number O of output parameters. However, the use of parameters passing into allocation instructions by Murphy is disclosed (see Murphy Appendix, col 91-94, *Allocate_Locale (Reg2)* pg. 8-9). Further, in a method to provide compiler-generated code with instructions set to provide register use and optimization as by Hastings; and to address complex floating-point operations as by Murphy (see

Art Unit: 2124

Murphy Appendix col. 53-54, table 6), Jarp discloses allocation instructions having input registers, local registers, and output registers (e.g. pg. 7, 8, 16). Official notice is taken that the efficient use of registers being indispensable in system where the number of available processor architecture registers is limited was a well-known concept in the art at the time the invention was made. It would have been obvious for an ordinary skill in the art at the time of the invention was made to implement the allocation instructions as suggested by Hastings and further enhanced by Murphy so as to provide parameters passed to such instructions as suggested by Jarp because the status of the registers being used as input registers, local registers, and output registers to associate data change in conjunction with procedure call/return in the stack context as taught by Hastings would be beneficial and needed information as to how registers have been used so to provide efficient register reuse in view of the well-known concept to optimize the use of registers (e.g. Hastings, *Allocate/Deallocate* – Fig. 6).

As per claim 3, Hastings in combination with Murphy teaches the creation of a modified set of registers based on call to reallocate stack memory (re claim 1) but does not explicitly disclose modifying the number O of the parameters to generate the number O of the new parameters; but in view of the rationale from the rejection in claim 2, this limitation would have been obvious because the step of providing allocation instructions with specific input, output parameters as taught by Jarp would have met the required O number of new parameters.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat No. 5,564,031 to Amerson et al., disclosing deallocating of registers for reuse.

U.S. Pat No. 4,777,588 to Case et al., disclosing reuse of procedural registers.

Art Unit: 2124

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please consult Examiner before using this number)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. , 22202. 4th Floor(Receptionist).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

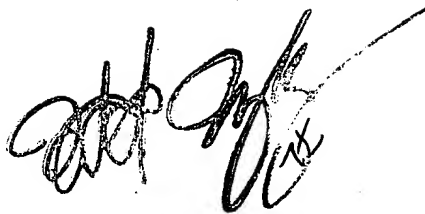
VAT

Application/Control Number: 09/765,931

Page 6

Art Unit: 2124

March 4, 2004

A handwritten signature in black ink, appearing to read 'Todd Ingberg', with a long horizontal flourish extending to the right.

Todd Ingberg
Primary Examiner
Group 2100